Improving Circuit Designs with Worst Case Logic Compatibility Analysis

By Charles Hymowitz, Sahar Sadeghi, AEi Systems

Abstract—Digital worst case Logic Compatibility analysis computes the worst case DC interface compatibility for the entire design. The goal is to demonstrate positive margins for the required input voltages Vih and Vil, positive margins for the worst case load currents seen by the drivers, and margins for the recommended fan-out of the drivers. In this article, the results of a design analyzed using AEi Systems' automated Logic Command software are presented.

I. INTRODUCTION

Worst Case Circuit Analysis ('WCCA') is a cost-effective means of screening a design to verify, with a high degree of confidence, that potential defects and deficiencies are identified and eliminated prior to test, production, and delivery and that the design will function, within specifications, throughout its lifetime. The digital worst case logic interface compatibility analysis portion of a comprehensive WCCA analyzes 100% of the design in order to verify that the digital ICs can reliably drive the correct logic levels to all destinations and meet all of the input requirements under worst case conditions. The goal is to demonstrate positive margins for the required input voltages Vih and Vil, positive margins for the worst case load currents seen by the drivers, and margins for the recommended fan-out of the drivers.

At AEi Systems' interface compatibility analysis is performed using our proprietary Logic Command software which combines both HyperLynx and SPICE simulation in an automated fashion. All required electrical information, for each net, is automatically extracted from various sources including HyperLynx. The information includes net connectivity, trace properties, peak crosstalk from switching on nearby traces, I/O characteristics and pertinent requirements. The information is converted into a SPICE netlist describing the source, path, and load. Initially, a sensitivity analysis is used to determine the worst case combination of all of the component tolerances. Once the sensitivities are known, the updated SPICE file is rerun again to determine the worst case voltages and currents at all related I/Os. The software also compiles the reports and associated summary data tables greatly speeding the assessment. This is a critical factor given digital designs can have hundreds or thousands of nets each with many sources and load combinations.

Analysis of only "critical" nets is not sufficient, especially for high reliability systems. Many problems, as discussed in the conclusions below, are missed if 100% of the design is not analyzed.

Figure 1 shows the block diagram of the AEi Systems' proprietary in-house Logic Command software.

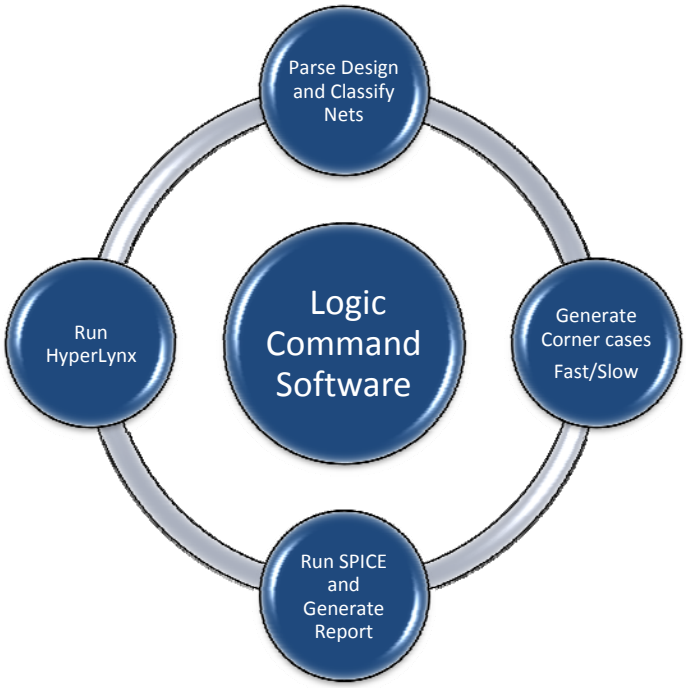

Figure 1: AEi Systems proprietary Logic Command software includes signal integrity analysis, crosstalk, and DC interface compatibility analysis.

II. DIGITAL WORST CASE DC INTERFACE COMPATIBILITY EXAMPLE

A portion of an actual analysis is shown below. The output of the analysis easily shows if the digital ICs drive the correct logic levels to all receivers and meet the entire input requirement under the worst case conditions of initial, temperature, aging, and radiation tolerances.

Digital systems often contain a large number of signals used for communication between several types of digital ICs. The IC's inputs and outputs ('I/Os') are connected in many combinations with a variety of fanouts, signaling standards and requirements. Performing manual analysis by hand, individually, for thousands of nets with multiples cases (fast – slow drivers, etc.) usually takes several months. AEi Systems' Logic Command software significantly reduces the analysis time by over an order of magnitude.

The digital nets are broken down into single-ended input-only nets, differential one-directional nets, single-ended bi-directional nets, no connected nets, differential inputs only, Tri-stateable differential I/Os, Tri-stateable single-ended I/Os for easier assessment and documentation grouping.

III. WORST CASE DC INTERFACE COMPATIBILITY ANALYSIS PROCESS

Figure 2 shows an example of the simulation of a single-ended output and one or more single ended inputs. The output in these nets is capable of driving both logic 'Low' and logic 'High' levels, but is not capable of

going into the Hi-Z state. The analysis verifies sufficient margin for Vih and Vil of every input. Since there are two possible states, each net is analyzed for two cases: 'HIGH' and ‘LOW’.

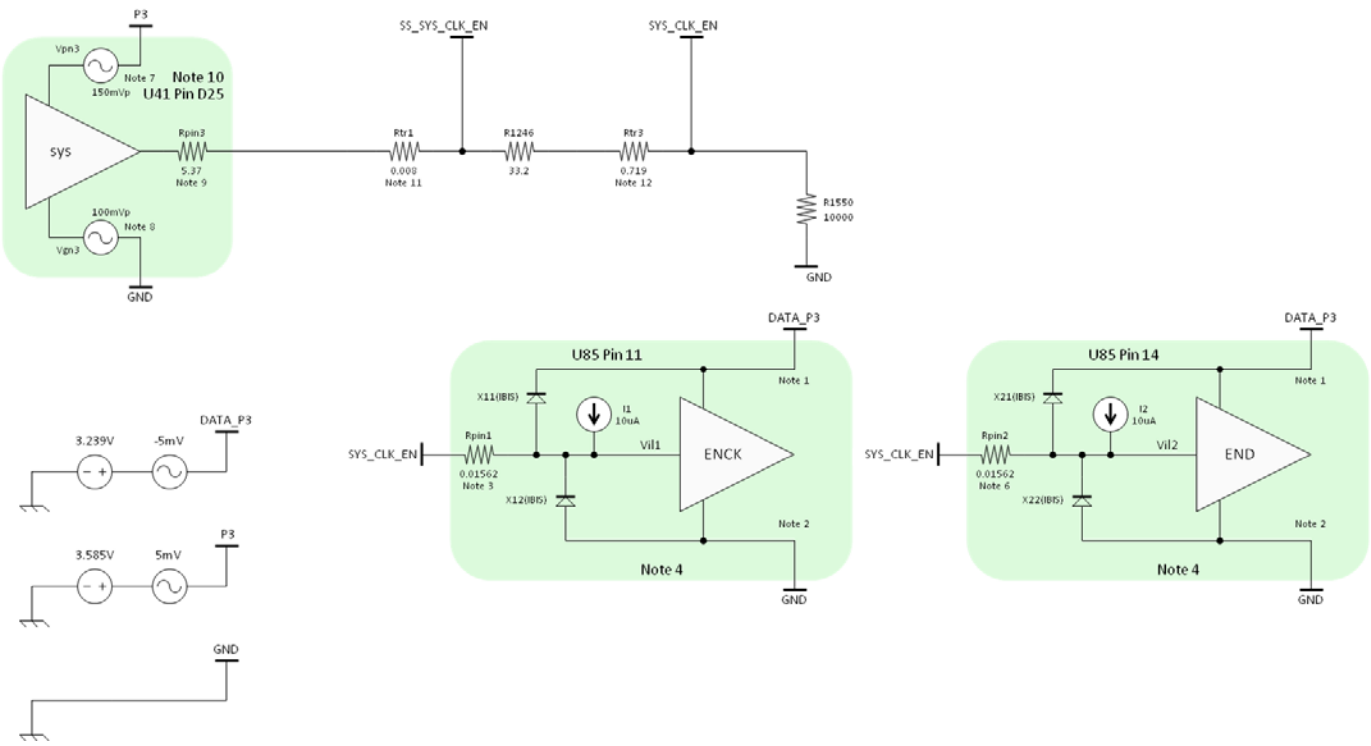

Figure-2: The specified nets in Logic High State Circuit Diagram.

For this analysis, it is assumed that there is no internal Vdd or ground noise. It is also assumed that the amount of VDD noise from other sources is limited to +/- 150mV and the ground bounce is limited to +/- 100mV. These assumptions can be modified to the exact specification of the design and the program’s environment. The power supply limits are usually taken from the analog worst case analysis results.

The information depicted in the figure above is used to generate the SPICE netlist for each set of sensitivity tolerances for every calculated result. One of the simulation files is provided below as an example. Again, the generation, simulation, and data gathering from the simulation output results are all automated.

```
NET SYS_CLK_EN VOH ANALYSIS. CASE#6. TOLERANCES SET TO MAX.
* FILE NAME: SYS_CLK_EN.SP
.LIB IBIS.LIB
* NO INTERNAL SUPPLY NOISE SOURCE FOR U85
* NO INTERNAL GROUND NOISE SOURCE FOR U85
RPIN1 CLK_EN VIH1 0.01562     ; MAXIMUM PIN DC RESISTANCE
X11 VIH1 N3 INPUT_3.3V_15_UCLAMP_MAX
X12 VIH1 N2 INPUT_3.3V_15_LCLAMP_MAX
* PIN U85.11 HAS NO INTERNAL PULL-UP/DOWN
```

```
I1 N3 VIH1 0.00001 LOAD    ; INPUT LEAKAGE CURRENT OUT OF U85.11
* NO INTERNAL SUPPLY NOISE SOURCE FOR U85
* NO INTERNAL GROUND NOISE SOURCE FOR U85
RPIN2 SYS_CLK_EN VIH2 0.01562     ; MAXIMUM PIN DC RESISTANCE
X21 VIH2 N3 INPUT_3.3V_15_UCLAMP_MAX
X22 VIH2 N2 INPUT_3.3V_15_LCLAMP_MAX
* PIN U85.14 HAS NO INTERNAL PULL-UP/DOWN
I2 N3 VIH2 0.00001 LOAD    ; INPUT LEAKAGE CURRENT OUT OF U85.14
VPN3 VCC3 N8 0.15    ; SUPPLY NOISE INSIDE U41
VGN3 VSS3 N2 -0.1    ; GROUND NOISE INSIDE U41
RPIN3 VOH1D VOH1 5.37     ; MAXIMUM DRIVER PIN DC RESISTANCE
* OUTPUT DRIVER MODEL. DRIVING LOGIC HIGH.
X33 VOH1D VCC3 TTL3H1_OUT_108_PULLUP_MAX     ; IBIS PULL-UP MODEL FOR U41.D25
VX1969 VOH1 VOH1R 0     ; NO CROSSTALK ON NET SS_ _SYS_CLK_EN
RTR2 VOH1R SS_ _SYS_CLK_EN 0.008     ; RESISTANCE OF TRACE
R1246 SS _SYS_CLK_EN SS_CLK_ENR1 34.43172     ; RESISTANCE OF ON-BOARD PART R1246
RTR4 SS_SYS_CLK_ENR1 SYS_CLK_EN 0.719     ; RESISTANCE OF TRACE
R1550 SYS_CLK_EN N2 10371     ; RESISTANCE OF ON-BOARD PART R1550
VDD3 NX3 0 3.585     ; DC POWER SOURCE FOR DATA_P3D3V NET
VDN3 N3 NX3 0.005     ; AC PEAK RIPPLE ON POWER SOURCE FOR DATA_P3D3V NET
VDD8 NX8 0 3.585     ; DC POWER SOURCE FOR p3 NET
VDN8 N8 NX8 0.005     ; AC PEAK RIPPLE ON POWER SOURCE FOR p3 NET
VSS2 NX2 0 0     ; DC GROUND OFFSET FROM CHASSIS TO GND NET
VDN2 N2 NX2 0     ; AC PEAK RIPPLE ON RETURN NET GND NET
.OP
.END
```

The SPICE simulation result including the appropriate requirements and worst case margin are as follows:

Element	Param	Node	Node Ref.	Units	Req. Min	Req. Max	Min	Max	Margin	P/F	SPICE File Min Case	SPICE File Max Case	Notes
U85.11	Vcc	V(n3)	V(n2)	Volts	3	3.6	3.234	3.59	0.01	PASS	1020.sp	1025.sp	Supply voltage range
U85.11	Vih	V(vih1)	V(n2)	Volts	2	5.59	3.053	3.717	1.053	PASS	1021.sp	1026.sp	Logic High Input Voltage
U85.14	Vcc	V(n3)	V(n2)	Volts	3	3.6	3.234	3.59	0.01	PASS	1020.sp	1025.sp	Supply voltage range
U85.14	Vih	V(vih2)	V(n2)	Volts	2	5.59	3.053	3.717	1.053	PASS	1022.sp	1027.sp	Logic High Input Voltage
U41.D25	Ioh	I(Rpin3)		mA	0	8	0.375	0.499	7.501	PASS	1023.sp	1028.sp	Max Output Current High (Absolute Value)
U41.D25	Vcc	V(vcc3)	V(vss3)	Volts	3	3.6	2.984	3.84	-0.24	FAIL	1024.sp	1029.sp	Supply voltage range

Table-1: The simulation results of six cases of all the applicable requirements for all the elements on these two nets are shown in this table. The supply voltage range is failed with -0.24V margin.

After the interface compatibility between digital ICs on a sample board was exhaustively analyzed, the following issues were identified.

1. The supply voltage provided for this design has a rather high maximum limit of 3.6V with the ripple of 15mVpp resulting in the peak voltage of 3.615V. The maximum operational for all parts are 3.6V

maximum. The DC margin does not leave any room to absorb any load-induced AC effects such as plane noise and SSO[1].

2. AEi Systems' Logic Command software has ability to detect all the floating pins, and copper traces of design. For this design, the software detected several floating traces. Floating metal with a large cross-sectional area can result in an IESD discharge to surrounding traces upsetting or damping flight parts. Lastly, this design has a number of signals driven by a tri-stateable buffer into an FPGA. That would result in floating inputs when the driver is in HiZ.

Design issues can be easily identified via worst case interface compatibility analysis. Issues that cause data corruption, anomalous operation, and even product failure can be uncovered and fixed. The performance of such analyses creates many 'lessons learned' for designers. Not only are current designs improved but WCCA supports CIPs (Continuous Improvement Plans) resulting in better future products and better engineers.

Sample reports are available at http://www.aeng.com/signal.htm.

[1] http://www.aeng.com/AEi publications/Power Integrity/SSO Noise Effects in RTAX FPGAs-Part1